EXHIBIT 14

Electronic Acknowledgement Receipt

EFS ID:	40871572
Application Number:	16391151
International Application Number:	
Confirmation Number:	3694
Title of Invention:	MEMORY MODULE WITH TIMING-CONTROLLED DATA BUFFERING
First Named Inventor/Applicant Name:	Hyun Lee
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Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	129980-5049-US01
Receipt Date:	16-OCT-2020
Filing Date:	22-APR-2019
Time Stamp:	23:29:49
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment after Notice of Allowance (Rule 312)	129980-5049-US01_312_AMEND.pdf	124106 d053362e94b42ef41de42a9c9ab77388a925b827	no	11

Warnings:

Information:	
Total Files Size (in bytes):	124106

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New International Application Filed with the USPTO as a Receiving Office

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Electronically filed October 16, 2020

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun Lee et al.	Confirmation No.:	3694
Serial No.:	16/391,151	Art Unit:	2183
Filed:	April 22, 2019	Examiner:	Sun, Michael
For:	*MEMORY MODULE WITH TIMING-CONTROLLED DATA BUFFERING*	Attorney Docket No.:	129980-5049-US01

AMENDMENT UNDER 37 C.F.R. § 1.312

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The enclosed Amendment is filed after a Notice of Allowance dated July 23, 2020, and is filed under 37 C.F.R. § 1.312.

The Commissioner is hereby authorized to charge any required fee(s) to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5049-US01).

Amendments to the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Cancelled)

2. (Currently Amended) A memory module operable in a computer system to communicate with a memory controller of the computer system via a memory bus including control and address (C/A) signal lines and a data bus, the memory module comprising:

a module board having edge connections to be coupled to respective signal lines in the memory bus;

a module control device on the module board configurable to receive input C/A signals corresponding to a memory read operation via the C/A signal lines and to output registered C/A signals in response to the input C/A signals and to output module control signals;

memory devices arranged in multiple ranks on the module board and coupled to the module control device via module C/A signal lines that conduct the registered C/A signals, wherein the registered C/A signals cause a selected rank of the multiple ranks to perform the memory read operation by outputting read data and read strobes associated with the memory read operation, and wherein a first memory device in the selected rank is configurable to output at least a first section of the read data and at least a first read strobe; and

data buffers on the module board and coupled between the edge connections and the memory devices, wherein a respective data buffer of the data buffers is coupled to at least one respective memory device in each of the multiple ranks and is configurable to receive the module control signals from the module control device, and wherein a first data buffer of the data buffers is coupled to the first memory device and is configurable to, in response to one or more of the module control signals:

delay the first read strobe by a first predetermined amount to generate a first delayed read strobe;

sample the first section of the read data using the first delayed read strobe; and

transmit the first section of the read data to a first section of the data bus;

wherein the first predetermined amount is determined based at least on signals received by the first data buffer during one or more previous operations ~~before the memory read operation~~.

3. (Currently Amended The memory module of claim 2, wherein a second memory device in the selected rank is configurable to output at least a second section of the read data and at least a second read strobe, and wherein the data buffers further include a second data buffer configurable to, in response to the one or more of the module control signals:

delay the second read strobe by a second predetermined amount to generate a second delayed read strobe;

sample the second section of the read data using the second delayed read strobe; and

transmit the second section of the read data to a second section of the data bus;

wherein the second predetermined amount is determined based at least on signals received by the second data buffer during one or more previous operations ~~before the memory read operation~~.

4. (Currently Amended) The memory module of claim 3, wherein a third memory device in the selected rank is configurable to output a third section of the read data and a third read strobe, wherein each of the first section, the second section, and the third section of the read data is 4-bit wide, and wherein the first data buffer is further coupled to the third memory device and is further configurable to, in response to the one or more of the module control signals:

delay the third read strobe by a third predetermined amount to generate a third delayed read strobe;

sample the third section of the read data using the third delayed read strobe concurrently with sampling the first section of the read data using the first delayed read strobe; and

transmit the third section of the read data to a third section of the data bus concurrently with transmitting the first section of the read data to the first section of the data bus;

wherein the third predetermined amount is determined based at least on signals received by the first data buffer during one or more previous operations ~~before the memory read operation~~.

5. (Currently Amended) The memory module of claim 3, wherein the signals received by the first data buffer ~~before the memory read operation includes~~ during one or more previous operations include at least a strobe signal associated with a previous operation, and wherein the signals received by the second data buffer ~~before the memory read operation includes~~ during one or more previous operations include at least another strobe signal associated with the previous operation.

6. (Previously Presented) The memory module claim 3, wherein each of the first section and the second section of the read data is 4-bit wide, and wherein the at least one respective memory device in each of the multiple ranks includes one memory device having a bit width of 8 or two memory devices each having a bit width of 4.

7. (Currently Amended) The memory module of claim 2, wherein the signals received by the first data buffer ~~before the memory read operation includes~~ during one or more previous operations include at least a strobe signal associated with a previous operation.

8. (Previously Presented) The memory module of claim 2, wherein the module control device is further configurable to receive a system clock signal and output a module clock signal, and wherein the first data buffer is further configurable to:

receive the module clock signal;

generate a local clock signal having a programmable phase relationship with the module clock signal; and

output the local clock signal;

wherein the first memory device is configurable to receive the local clock signal and to output the first section of the read data and first read strobe in accordance with the local clock signal.

9. (Previously Presented) The memory module of claim 2, wherein the module control device is further configurable to receive a system clock signal and output a module clock signal together with the module control signals to the data buffers, and wherein the first data buffer further includes receiver circuits corresponding to respective ones of the module control signals,

a respective receiver circuit for a respective module control signal including a metastability detection circuit configurable to generate one or more metastability indicators indicating a metastability condition in the respective module control signals with respect to the module clock signal.

10. (Previously Presented) The memory module of claim 9, wherein the metastability detection circuit is further configurable to generate at least one delayed version of the module clock signal, and at least one delayed version of the respective module control signal, and wherein the respective receiver circuit further includes a signal selection circuit configurable to receive the module clock signal and the at least one delayed version of the module clock signal, and to select a clock signal from among the module clock signal and the at least one delayed version of the module clock signal based on at least a first metastability indicator of the one or more metastability indicators.

11. (Previously Presented) The memory module of claim 10, wherein the signal selection circuit is further configurable to receive the respective module control signal and the at least one delayed version of the respective module control signal, and to select a module control signal from among the respective module control signal and the at least one delayed version of the respective module control signal based at least on a second metastability indicator of the one or more metastability indicators; and wherein the respective receiver circuit further includes a sampler that samples a selected module control signal according to a selected module clock signal and outputs received respective module control signal.

12. (Currently Amended) The memory module of claim 2, wherein the first data buffer includes circuitry that determines the first predetermined amount based at least on the signals received by the first data buffer during one or more previous operations ~~before the memory read operation~~.

13. (Previously Presented) The memory module of claim 2, wherein the first section of the read data is 4-bit wide, and wherein the at least one respective memory device in each of the

multiple ranks includes one memory device having a bit width of 8 or two memory devices each having a bit width of 4.

14. (Previously Presented) The memory module of claim 2, wherein the memory devices are selected from the group consisting of dynamic random-access memory, synchronous dynamic random-access memory, and double-data-rate dynamic random-access memory.

15. (Previously Presented) A method, comprising:

at a memory module in a computer system and operable to communicate data with a memory controller of the computer system via a memory bus including control and address (C/A) signal lines and a data bus, the memory module including a module board having edge connections to be coupled to respective signal lines in the memory bus, a module control device on the module board, memory devices arranged in multiple ranks on the module board and coupled to the module control device, and data buffers on the module board and coupled between the edge connections and the memory devices, the data buffers including a first data buffer, wherein each respective data buffer is coupled to one respective memory device having a bit width of 8 or two respective memory devices each having a bit width of 4 in each of the multiple ranks;

receiving, at the module control device, input C/A signals corresponding to a memory read operation via the C/A signal lines;

outputting, at the module control device, registered C/A signals in response to the input C/A signals, wherein the registered C/A signals cause a selected rank of the multiple ranks to perform the memory read operation by outputting read data and read strobes associated with the memory read operation, and wherein a first memory device in the selected rank is coupled to the first data buffer and is configurable to output at least a first section of the read data and at least a first read strobe;

outputting, at the module control device, module control signals;

receiving, at each of the data buffers, the module control signals from the module control device;

the method further comprising, at the first data buffer, in response to one of more of the module control signals:

delaying the first read strobe by a first predetermined amount to generate a first delayed read strobe;

sampling the first section of the read data using the first delayed read strobe; and

transmitting the first section of the read data to a first section of the data bus; and

the method further comprising, before receiving the input C/A signals corresponding to the memory read operation at the module control device, determining the first predetermined amount based at least on signals received by the first data buffer.

16. (Currently Amended) The method of claim 15, wherein the data buffers further include a second data buffer, and wherein a second memory device in the selected rank is coupled to the second data buffer and is configurable to output at least a second section of the read data and at least a second read strobe, the method further comprising, at the second data buffer, in response to the one or more of the module control signals:

delaying the second read strobe by a second predetermined amount to generate a second delayed read strobe;

sampling the second section of the read data using the second delayed read strobe; and

transmitting the second section of the read data to a second section of the data bus;

wherein the second predetermined amount is determined based on signals received by the second data buffer during one or more previous operations ~~before the memory read operation~~.

17. (Currently Amended) The method of claim 16, wherein a third memory device in the selected rank is coupled to the first data buffer and is configurable to output a third section of the read data and a third read strobe, the method further comprising, at the first data buffer, in response to the one or more of the module control signals:

delaying the third read strobe by a third predetermined amount to generate a third delayed read strobe;

sampling the third section of the read data using the third delayed read strobe concurrently with receiving the first section of the read data using the first delayed read strobe; and

transmitting the third section of the read data to a third section of the data bus concurrently with transmitting the first section of the read data to the first section of the data bus;

wherein the third predetermined amount is determined based on the signals received by the first data buffer during one or more previous operations ~~before the memory read operation~~.

18. (Currently Amended) The method of claim 16, wherein the signals received by the first data buffer ~~before the memory read operation includes~~ during one or more previous operations include at least a strobe signal associated with a previous operation, and the signals received by the second data buffer ~~before the memory read operation includes~~ during one or more previous operations include at least another strobe signal associated with the previous operation.

19. (Previously Presented) The method of claim 15, further comprising:

receiving, at the module control device, a system clock signal concurrently with receiving the input C/A signals;

outputting, at the module control device, a module clock signal concurrently with outputting the module control signal;

receiving, at the first data buffer, the module clock signal;

generating, at the first data buffer, a local clock signal having a programmable phase relationship with the module clock signal; and

outputting, at the first data buffer, the local clock signal;

receiving, at the first memory device, the local clock signal; and

outputting, at the first memory device, the first section of the read data and first read strobe in accordance with the local clock signal.

20. (Previously Presented) The method of claim 15, further comprising:

receiving, at the module control device, a system clock signal concurrently with receiving the input control and address signal;

outputting, at the module control device, a module clock signal concurrently with outputting the module control signal;

generating, at the first data buffer, one or more metastability indicators indicating a metastability condition in a respective module control signal of the module control signals with respect to the module clock signal.

21. (Previously Presented) The method of claim 20, further comprising, at the first data buffer:

generating at least one delayed version of the module clock signal, and at least one delayed version of the respective module control signal;

selecting a clock signal from among the module clock signal and the at least one delayed version of the module clock signal based on at least one of the metastability indicators;

selecting a module control signal from among the respective module control signal and the at least one delayed version of the respective module control signal based at least on another metastability indicator; and

sampling the selected module control signal according to the selected module clock signal to output received respective module control signal.

REMARKS

This amendment is filed under 37 C.F.R. § 1.312 after the Notice of Allowance dated July 23, 2020.

REMARKS CONCERNING INFORMATION DISCLOSURE STATEMENT

Applicant appreciates Examiner's diligent review of the Information Disclosure Statement submitted on January 8, 2020 (IDS). In the Notice of Allowance, the Examiner notes that "in the IDS filed 1/08/2020 there were many Non-Patent Literature Documents and Foreign Patent Documents that were listed throughout without any corresponding copy of these documents attached." Applicant would like to point out that the IDS identified several related applications in which the references have been submitted, including applications to which the present application claims priority under 35 U.S.C. §120 ("the parent applications"), and a co-pending U.S. Patent Applications No. 15/470,856, filed on March 27, 2017 ("the co-pending application").

Applicant apologizes for mistakenly grouping the co-pending application in the IDS as one of the applications to which the present application claims priority under 35 U.S.C. §120. The co-pending application is instead an application that claims priority to a related application cross-referenced in the present application (i.e., U.S. Pat. App. No. 13/970,606, filed on August 20). The references in the IDS that are crossed out in the Notice of Allowance were listed in the IDS mainly due to the reason that they had been listed in Information Disclosure Statements in the co-pending application.

REMARKS CONCERNING CLAIMS

Claims 2-5, 7, 12, and 16-18 have been amended to address minor issues of clarity and to correct grammatical errors.

No new matter has been added, and the amendment should not necessitate additional search or examination. Therefore, entry of the amendment is respectfully requested.

With respect to all amendments, Applicant has not dedicated or abandoned any unclaimed subject matter. Moreover, Applicant has not acquiesced to any characterizations of the invention, nor any rejections or objections of the claims, made by the Examiner. Moreover,

the Applicant hereby rescinds any prior disclaimer of claim scope, to the extent they exist, made during the prosecution of this application or made during the prosecution of any patent or other related patents/applications, and advises the Examiner that any such previous disclaimers and the cited references that they were made to avoid may need to be revisited.

After entry of this amendment, the pending claims are: claims 2 - 21.

The Examiner is invited to call the undersigned attorney at (650) 521-4828, if a telephone call could help resolve any remaining items.

Respectfully submitted,

Date: October 16, 2020

/Jamie J. Zheng/ 51,167

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